

Requested Patent: JP63128736  
Title: SEMICONDUCTOR ELEMENT  
Abstracted Patent: JP63128736  
Publication Date: 1988-06-01  
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Application Number: JP19860274173 19861119  
Priority Number(s):  
IPC Classification: H01L23/04 ; H01L23/28 ; H01L23/32 ; H01L23/52 ; H01L25/08  
Equivalents:

**ABSTRACT:**

**PURPOSE:** To dispose a plurality of semiconductor chips in three dimensions on a loading substrate and to decrease a required area per one chip so that chip board composition of high mounting density can be realized, by fixing a first semiconductor chip on a loading substrate and disposing a second semiconductor chip in three dimensions on the first semiconductor chip and connecting the respective semiconductor chips with respective conductive patterns on the loading substrate and sealing the respective semiconductor chips.

**CONSTITUTION:** A first semiconductor chip 2 is fixed on a loading substrate 1, which consists of ceramics and glass-epoxy resin and the like, by die bonding. Bonding pads of the chip 2 are connected with conductive patterns, which are formed on the loading substrate 1, by the use of bonding wires 3, and next a cap 4 is put and stuck on the substrate 1 so as to seal the substrate 1. Bonding pads of a second semiconductor chip 5 fixed on the cap 4 are connected with the conductive patterns on the substrate 1 by the use of bonding wires 6. Sealing resin of a polyimide group is potted to entirely seal the cap 4, which seals the first semiconductor chip 2, and the second semiconductor chip 5 mounted on the cap 4.